A GaN-based Power Amplifier Module Design for 5G Base Stations

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***Abstract*—This paper presents a compact Power Amplifier Module (PAM) with class-AB topology designed for new-generation cellular base stations. The center frequency of 3.5GHz PAM is designed to target 5G New Radio (NR) and Long Term Evolution (LTE) bands. The module combines lumped element-based input, output matching networks, and a Gallium Nitride (GaN) High Mobility-Electron Transistor (HEMT) die, making it a hybrid design. The module was designed on a Rogers4003C laminate of 8.5 x 5.2 mm. Full-laminate layout electromagnetic analysis and vendor-supplied compact GaN device models are used in co-simulations to check the design's small signal and large signal behavior. The output power is tuned to 37.1 dBm with 39% power added efficiency(PAE). The transducer power gain is 12.4 dB, while the input and output return losses are -11.7 dB and -6.4 dB, respectively. Besides the small signal stability analysis, the large signal conditions are investigated to ensure unconditional stability up to the maximum oscillation frequency of the device.**

Keywords—Gallium nitride HEMT, LTE band 42, 5G n78, power amplifier module

I. INTRODUCTION

As the new generation of mobile services utilizes Multiple Input Multiple Output systems, the demand for power amplifiers is tremendously increased. There is a high demand for more power-efficient and cost-effective power amplifier modules. The increased data traffic and new frequency band additions require new cellular base stations to be more compact with higher performance. Moreover, the Microcells, Picocells, and Femtocells which are small-cell base stations, drew interest over macro cells as they emit less power, are more environmentally friendly, easier on thermal control, and smaller in size [1]. RF power amplifiers play an essential role in the transmitter design of cellular base stations. Since the microcells, picocells, and femtocells are smaller, their transmitter needs to be smaller and more efficient, which applies to power amplifiers.

GaN transistors have advantages over GaAs in the high energy band gap, allowing them to have higher power density and higher breakdown voltage [2]. As a result of higher breakdown voltage, GaN transistors can handle higher voltage swings and higher power outputs. In recent years there are many researches utilize the capabilities of the GaN transistor [3-5].In this work, class AB power amplifier module is designed with a GaN HEMT die transistor for compact base stations.

II. POWER AMPLIFIER DESIGN

This work aims to deliver 5W output power with a small module. The design goals are specified in Table (I). To achieve the design goals, the PAM's topology was selected as a hybrid module with a single die transistor and small discrete components on printed circuit board(PCB) laminate. The transistor selected Cree's CGH6008D GaN HEMT, a 0.8 x 0.9 mm die transistor. An 8W GaN HEMT was chosen for its capability of high power density, high breakdown voltage, broad bandwidth, and power output [6]. The mode of operation of PAM was chosen as class AB to balance the requirement of linearity and high power-added efficiency [7].

Furthermore, the non-linear transistor model of GaN HEMT CGH6008D was used to determine the bias point of operation. Fig. 1 shows the DC-IV curve of the chosen die HEMT. The bias point is selected as V_{gs}=-2.7V, which is the lower side of the load line. The chosen bias point of the PAM is supplied with V_{ds}=28V, which corresponds to the drain current of I_{ds}=0.134A. The GaN HEMT transistor model includes large signal characteristics, allowing harmonic balance simulations.

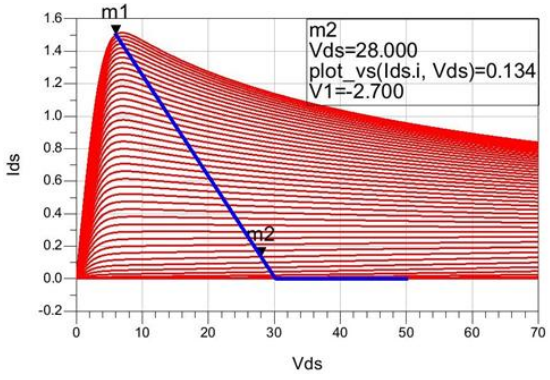

Fig. 1. DC-IV Curve of GaN HEMT CGH60008D.

TABLE I. DESIGN GOALS OF PAM

Design Goal	Value
Frequency	3.4-3.6 GHz
Output Power(dBm)	37
Power Added Efficiency	35%
Gain(dB)	12
Gain Compression(dB)	1
Module Size	10x6 mm

So, just like small-signal behavior, the load-pull simulations were done to develop the input and output matching networks based on the transistor's nonlinearity. The output matching network is designed using iterative load-pull and source-pull simulations to ensure optimum performance of the PAE and the 3rd order output Intercept Point (OIP3) for targeted power delivery [8]. The load-pull setup was prepared as shown in Fig. 2. Bias points were adjusted, as mentioned before. The source and load impedances for the maximum gain, the optimum OIP3 and the

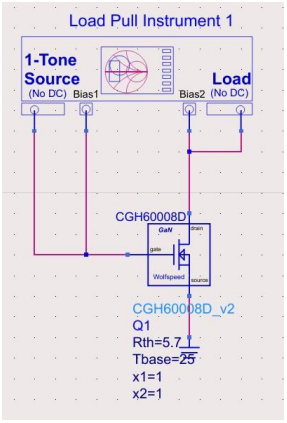

Fig. 2. Load Pull Setup for GaN HEMT Die Transistor

PAE for the transistor was found on the Smith Chart. At the optimum point selected in Fig 3, the source impedance is 0.58+j*5.92 Ω, and the load impedance is 18.68+j*28.19 Ω at the center frequency of the 3.4GHz-3.6GHz band for the 37 dBm output power. The contours indicate equal gain and matching PAE results. The marker was placed to gain contour to indicate an impedance value with the highest gain. This point gave a decent PAE result simultaneously, but it was not the highest PAE available. Typically, PAE has a peak value as the power approaches saturation value. However, one design goal was to gain compression to a maximum of 1 dB. So, the sweet spot was selected where both PAE and gain were satisfied.

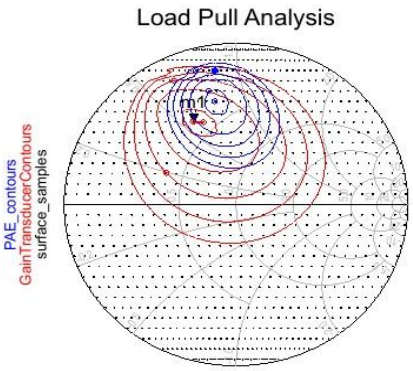

Fig. 3. Optimum Point on The Smith Chart from Load Pull Analysis

The HEMT die attached to the printed circuit board using the 25 µm gold bond wires for the gate and the drain connections. Bond wire effects were included in the design with the proper EM-based model where coupling among multiple wires and the ground plane and the mutual inductance are included [9]. Since the desired size is tiny for distributed elements at this frequency, the 0201 discrete lumped components were used for the power amplifier module design. The output matching was designed with a DC block capacitor and a low-pass LC network for harmonic suppression. The input matching network was built with a high pass T-network and stability network, and bond wire effects were included in the matching. The stability is ensured with a shunt RC at the gate of the transistor with a 100Ω.

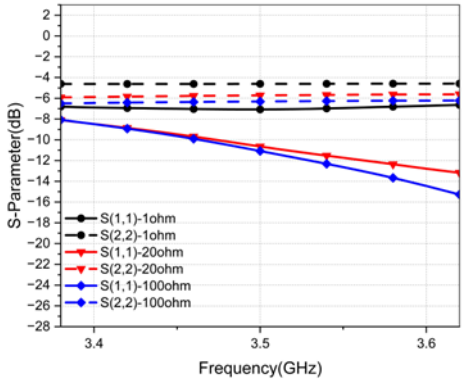

Fig. 4. Input and Output Return Loss Results for Altering Resistor Values

Different values of the resistor studied the determination of the resistor value. Fig. 4 indicates the input and output return loss values with the resistor change. Since the resistor value also modifies the matching network, a suitable value for the stability resistor was selected 100Ω for the better input and output return losses. After determining the stability resistor value, the layout was designed per the design goal of the total size. Fig. 5 shows the layout design of the PAM. 2-layer Rogers4003C laminate was selected for its high performance on high-frequency applications. Discrete lumped element packages and die transistor package was fit with careful floor planning, and conductor spaces were left for post-design optimization. The total size of the designed module is 8.5 x 5.2 mm.

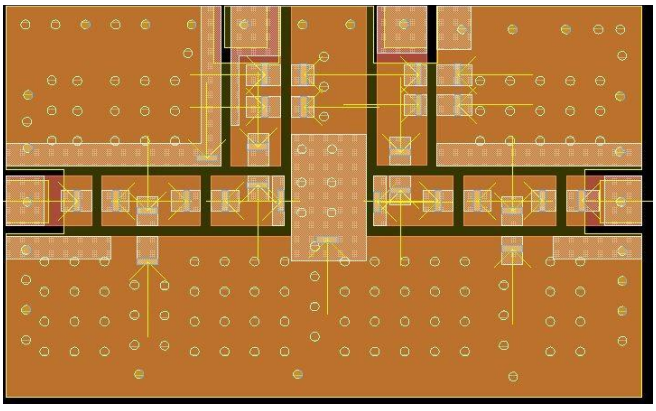

Fig. 5. . Designed Layout of PAM

Electromagnetic(EM) co-simulation of the designed layout was done with the real-life models of the discrete components, including the parasitic effects. Addition of layout parasitics and models of parts, matching networks were optimized, and the final circuit is shown in Fig. 6. Small signal and extensive signal simulations were performed after the design of the PAM.

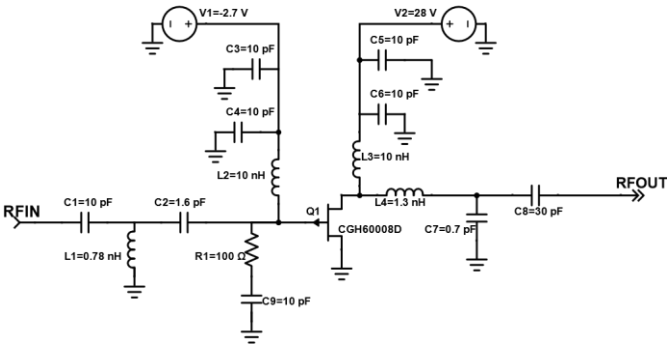

Fig. 6. Power Amplifier Module Schematic with Values

III. Simulation Results

A. Small Signal Simulation

The small signal of the PAM was analyzed. The input and output return losses were simulated with small signal gain. The power amplifier's input and output return losses are essential parameters since the amplified signal may damage the connected devices. Fig. 7 shows the S-parameter results of the designed PAM from DC-10 GHz. The simulated results of small signal gain are 13.8 dB, input return loss is -11.7 dB, and output return loss is -6.4 dB at 3.5 GHz. The frequency range of 3.4-3.6 GHz, as the design goal shows, the matching networks were designed appropriately.

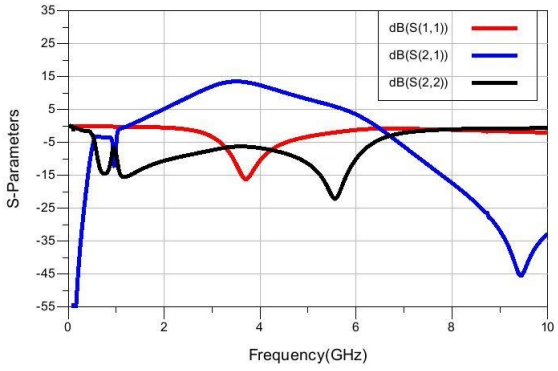

Fig. 7. Small Signal Results

As the maximum small signal gain and the desirable input-output return loss values, the small signal stability condition of the PAM was checked using μ and μ' stability criterion. The expected values of μ and μ' are above 1 for unconditional stability for a device. Fig. 8 indicates the small signal stability criteria μ and μ' from DC to 20 GHz. The chosen shunt resistor and capacitor values ensured the small-signal unconditional stability.

B. Large Signal Simulation

The power amplifiers are evaluated for their large-signal characteristics as they are used almost always under large-signal stimulation. The power amplifier; therefore, the large signal simulation was performed for the designed PAM. Fig. 9 shows the transducer power gain, PAE, and output power versus input power. Harmonic balance simulation results show that for the input power of 24.75 dBm, output power resulted in 37.1 dBm output power. PAE was 39%, and transducer power gain was 12.4 dB at the frequency of 3.5 GHz. The gain compression was around 1 dB.

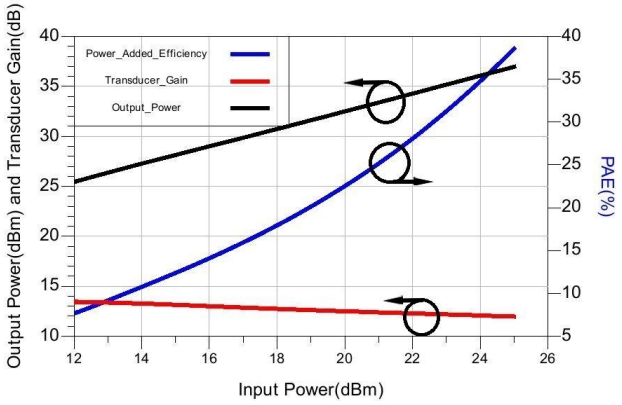

Fig. 9. Large Signal Results

Moreover, large-signal stability was checked. The large-signal stability was analyzed for an input power of 24.75 dBm. The loop gain is shown in (1). Considering an amplifier with an open loop gain of A, in real life, it has Feedback of β that comes from parasitic magnetic and electric couplings from the ground plane. The stability analysis can be made with the loop gain calculation [10].

$$A_f = \frac{A\beta}{1+A\beta} \quad (1)$$

The loop gain, $A\beta$, determines the stability with its value and phase. If the loop gain equals 1 with the phase of π degree, the system becomes unstable with the unrealistic A_f [11]. Loop gain was simulated for the PAM. For the output power of 5W, the loop gain simulation result is demonstrated in Fig. 10. Logarithmic result of loop gain was simulated for the drain and gate of the transistor. The maximum result of the logarithmic loop gain is around -18 dB from DC to 10 GHz, so the value of loop gain is lower than 1. This result ensures that large signal stability was granted.

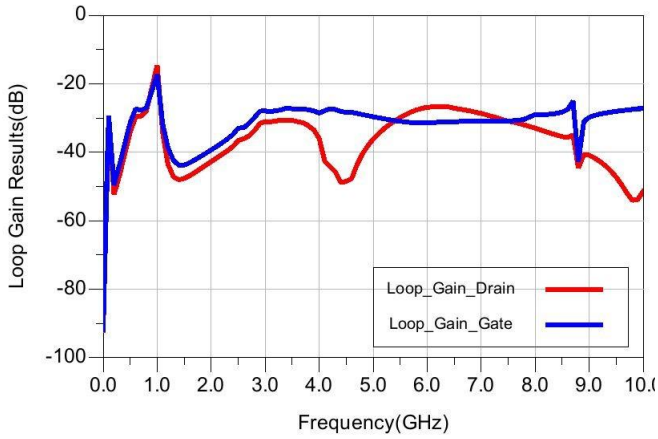

Fig. 10. Large Signal Loop Gain Result

TABLE II. PERFORMANCE COMPARISON OF RECENT GAN PAS

Ref.	Frequency(GHz)	Output Power(dBm)	Efficiency (%)	Size (mm^2)
[12]	3.6	40	40%	8x8
[13]	3.4–3.7	38.8	33 – 55%	4x2.5
[14]	3.0-3.6	34.2	45.9-50.2%	78x60
[15]	3.25	37.5	28%	3.5x2.8
This Work	3.4-3.6	37	39%	8.5x5.2

Table (II) shows a comparison of our work with the recent PAs.

IV. CONCLUSION

This work presents a compact hybrid power amplifier design with a GaN HEMT die, lumped, and distributed matching networks on a laminate. The amplifier is constructed as a class-AB single-stage topology with a low-pass output matching network and a high-pass input matching network in LC configuration. A shunt RC network is used at the input to increase stability. A parametric study of the resistor value is presented. The output power is simulated as 37.1 dBm with 39% PAE and 12.4 dB signal gain. The input return loss is -11.7 dB, and the output return loss is -6.4 dB at the center of the operating band, 3.5 GHz. The device is unconditionally stable across its working range. The design goals are achieved with a 1-stage 8.5 x 5.2 mm power amplifier module. The manufactured device prototype is being measured at the moment of this manuscript writing.

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